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OPTIMIZATION OF DIE-BONDING PROCESS USING ORTHOGONAL ARRAY EXPERIMENTS

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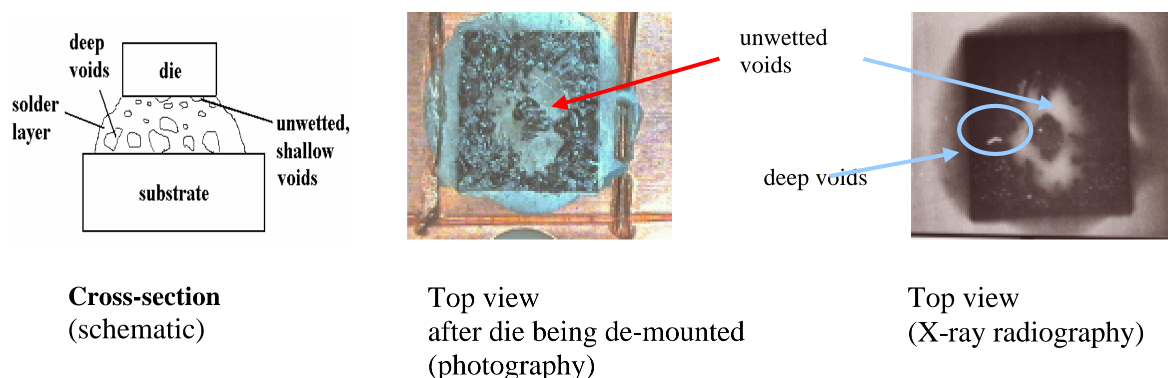
1. Introduction

Due to the functional requirements of heat dissipation, electrical conduction and mechanical strength (the ability to absorb stresses due to thermal expansion mismatch), soldering is usually used on the power devices such as power MOSFETs. Among the soft solders tin-lead (Sn-Pb) alloys are the most popular. While the solder melts in the bonding process, the oxide layer will be formed on the solder surface. To eliminate the oxide film, it is common to apply the scrubbing motion together with the reducing atmosphere in the bonding process.

In spite of the mentioned effort, the formation of solder voids is a troublesome problem, which reduces the localized thermal/electrical conductivity and mechnical strength, therefore lowers the reliability of power devices at service. Figure 1 shows some types of solder voids. The effects of solder voids, the packaging and assembly factors as well as the manufacturing variability affecting the die bonds have been studied by using numerical model, e.g. [Zhu 1999] or through experimental investigation, e.g. [Viduya 1996] [Evans 1998] [Radeck 2000]. The findings are instructive, but for many working forces in the production field, to shoot the on-line quality issues it seems they would choose other tools rather than the simulation based on the advanced mathematics or mechanics.

In this study, to reduce the voids in the bonding layer of power transistor, a small number of experiments using orthogonal arrays are conducted systematically, which give the optimum combination of process parameters under a specified range of die-bonding machine, above all, without resort to any advanced numerical simulation tools.



Cross-section
(schematic)

Top view
after die being de-mounted
(photography)

Top view
(X-ray radiography)

Figure 1. Schematic of the solder voids

2. Process

The target chip is a kind of power MOSFETs used for the switching purpose and packaged in the form coded as TO-3PFM [Hitachi 2001]. Figure 2 represents the assembly outline. As stated in the Table 1, the die with back metallization (Ti/Ni/Ag/Au) is bonded on the lead frame (Cu+Sn:? 99.96%) using the scrubbing method at a die bonder (Figure 3). The soft solder applied is Sn-Pb alloy (Sn:5.0%, Ag:2.5%, Pb:92.5%). At the entrance, the substrate is transported into the rail and heated up. The rail is divided, from the entrance end to the exit, into the preheating, processing and cooling zone, respectively. As illustrated in Figure 4, the solder is dispensed on the die pad, stretched evenly out and then the die is picked and mounted onto, all the three steps are performed in the middle of rail within the surrounding gas mixture. At the following section, the substrate cools down before exit.

In the past months before this study, voids appear in the bonding layer and reduce the reliability of the device. The average area of the voids measured by using the X-ray radiography amount to 9.3% of the examined surface, which lies beyond the accepted limit 7%. The troublesome situation must be resolved as soon as possible, and if available, any other methods than the numerical simulation tools would be recommended.

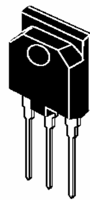


Figure 2. Package outline (TO-3PFM) for the power transistor

Table 1. Outline of devices used in the experiment

die	solder	substrate
Power MOS FET (for switching use) from silicon wafer with die back metallization first layer: Ti second layer: Ni third layer: Ag/Au	Sn: (5.0±1.0)? Ag: (2.5±1.0) ? Pb: 92.5 ?	Cu+Sn= 99.96 % Sn:(0.1~0.15) % Rest : Fe, P , O_2

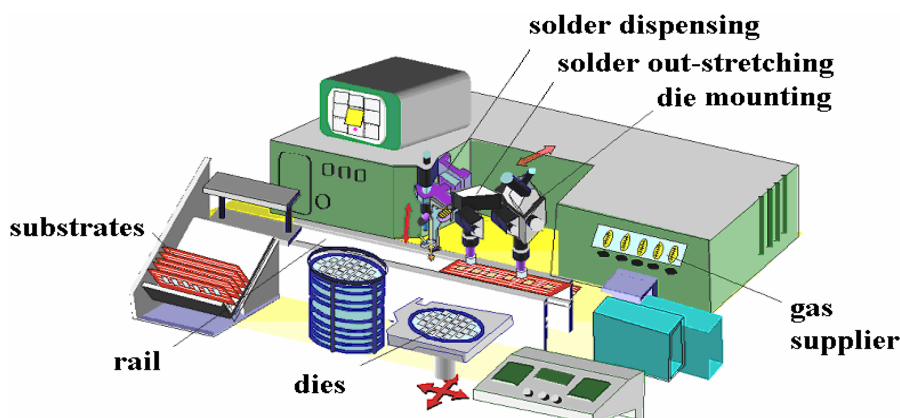
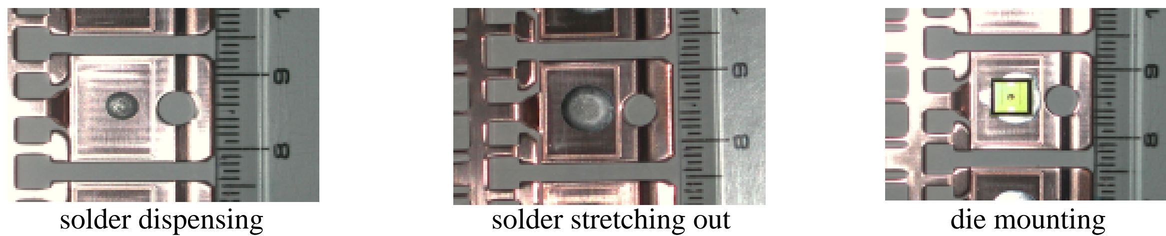


Figure 3. Schematic of a soft solder die bonder



solder dispensing　　solder stretching out　　die mounting

Figure 4. Illustration of the soft solder die bonding process

After discussion with the working group, the Taguchi method using the orthogonal arrays is decided. The use of the orthogonal arrays minimizes the number of trial experiments [Taguchi 1987] and makes it possible to realize the process redesign before the stringent deadline. The possible factors affecting the quality of die-bonding process, i.e. the process parameters that have influence on the quantity of solder voids, and their levels within the specified working range, are chosen (Figure 5). The process parameters include amount of solder, gas mixture, temperature set at the preheating zones, temperature of solder dispensed, mounting temperature, down speed of the bonder head, range, speed, motion type and duration of the scrubbing action etc., as shown in Table 2. The quality characteristic will be the smaller the better.

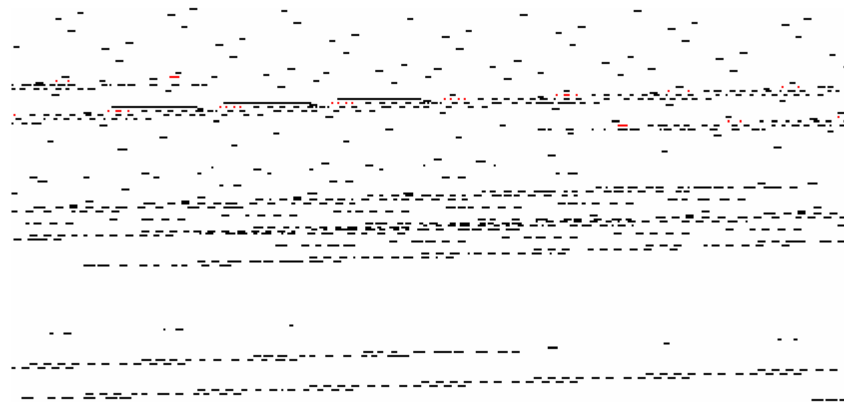


Figure 5. Cause and effect diagram for the voids in the solder bonds

Table 2. Factors and levels for the first screening run

Factor	A	B	C	D	E	F	G	H	I	J	K	L
Level	amount of solder	index of rail	scrub range	scrub speed	scrub motion type	scrub time	down speed	pre-heat 1	pre-heat 2	pre-heat 3	solder temp.	die mount temp.
1	45	250	10	2	1	1	5	285	270	330	360	405
2	47	300	20	4	2	2	10	315	300	350	380	425
3	50	350	30	6	4	3	15	345	330	370	400	445

3. Results

The full factorial experiments required to investigate all possible factor-level combinations will be too large to be practicable. Instead, a screening run of 27 trials arranged after the orthogonal array $\mathbf{L_{27}(3^{13})}$ is carried out first (Table 3), and the main factors are pinpointed through the analysis of response graph (Figure 6). For the first screening run, the settings of gas mixtures are considered as fixed and not taken into consideration. As shown in the Figure 6, the amount of solder (factor A), the scrubbing range (factor C), and the scrubbing time (factor F) play significant roles, while the variation

of the preheat settings makes little difference with respect to the reduction of solder voids. Then, a preliminary test under the selected factor-level combination i.e. $\mathbf{A_1}$ B_2 $\mathbf{C_2}$ $\mathbf{D_3}$ $\mathbf{E_3}$ $\mathbf{F_3}$ $\mathbf{G_3}$ $\mathbf{H_2}$ $\mathbf{I_3}$ $\mathbf{J_1}$ $\mathbf{K_1}$ $\mathbf{L_3}$ is repeated three times, 10 pieces of devices are taken each time. The amount of voids on the average reduces to 6.69% of the examined surface, but some still lies above 7%. Therefore, a secondary test with 6 main effects derived from the first run and the inclusion of 4 new parameters about the gas mixture, i.e. upper and lower streams at the location of solder dispensing and of die mounting, is conducted and the orthogonal array $\mathbf{L_{12}(2^{11})}$ is chosen . For each parameter now only 2 levels are considered. From the repeated experiments we found the voids on the average reduces to 3.19%, all within the accepted limit, but with some close to 7%, i.e. unstable.
Final test with 7 main effects is performed based on the foregoing results and the orthogonal array $\mathbf{L_8(2^7)}$. The amount of solder, scrubbing range, speed, motion type, time and down speed as well as the lower gas stream at the solder dispensing are the factors taken into consideration. The amount of voids on the average now drops to 1.73% of the measured surface, far below the accepted limit (Figure 7).

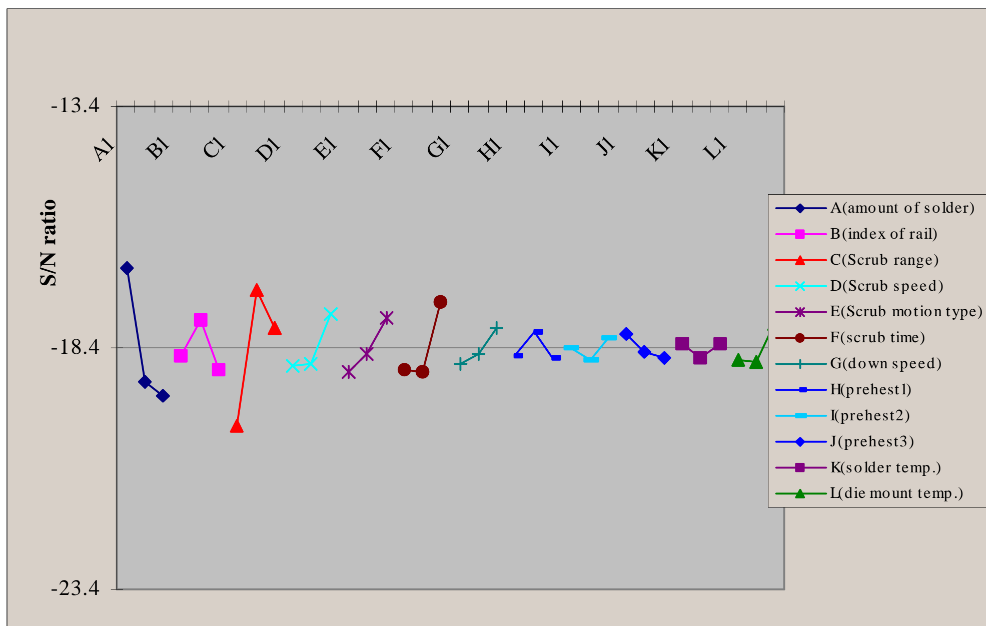


Figure 6. Response graphs for the first screening run

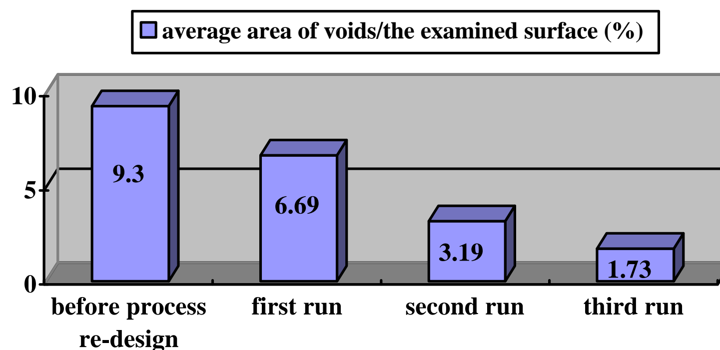
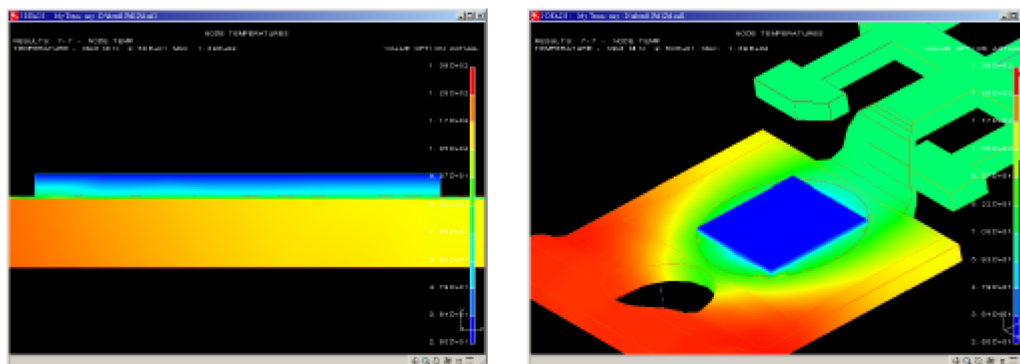


Figure 7. Average area of voids measured by using X-ray radiography

Table 3. Experiment layout with orthogonal array $L_{27}(3^{13})$ for the first screening run (27 trials for 13 factors with 3 levels)

Factor	A	B	C	D	E	F	G	H	I	J	K	L
Trial No.	amount of solder	index of rail	scrub range	scrub speed	scrub motion type	scrub time	down speed	pre-heat 1	pre-heat 2	pre-heat 3	solder temp.	die mount temp.
1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	2	2	2	2	2	2	2	2
3	1	1	1	1	3	3	3	3	3	3	3	3
4	1	2	2	2	1	1	1	2	2	2	3	3
5	1	2	2	2	2	2	2	3	3	3	1	1
6	1	2	2	2	3	3	3	1	1	1	2	2
7	1	3	3	3	1	1	1	3	3	3	2	2
8	1	3	3	3	2	2	2	1	1	1	3	3
9	1	3	3	3	3	3	3	2	2	2	1	1
10	2	1	2	3	1	2	3	1	2	3	1	2
11	2	1	2	3	2	3	1	2	3	1	2	3
12	2	1	2	3	3	1	2	3	1	2	3	1
13	2	2	3	1	1	2	3	2	3	1	3	1
14	2	2	3	1	2	3	1	3	1	2	1	2
15	2	2	3	1	3	1	2	1	2	3	2	3
16	2	3	1	2	1	2	3	3	1	2	2	3
17	2	3	1	2	2	3	1	1	2	3	3	1
18	2	3	1	2	3	1	2	2	3	1	1	2
19	3	1	3	2	1	3	2	1	3	2	1	3
20	3	1	3	2	2	1	3	2	1	3	2	1
21	3	1	3	2	3	2	1	3	2	1	3	2
22	3	2	1	3	1	3	2	2	1	3	3	2
23	3	2	1	3	2	1	3	3	2	1	1	3
24	3	2	1	3	3	2	1	1	3	2	2	1
25	3	3	2	1	1	3	2	3	2	1	2	1
26	3	3	2	1	2	1	3	1	3	2	3	2
27	3	3	2	1	3	2	1	2	1	3	1	3



Overview **Cross-section (enlarged)**

Figure 8. Thermal analysis of the solder bond using finite element method (I-DEAS)

4. Conclusion

Optimization of die-bonding process using orthogonal array experiments is performed without any introduction of numerical simulation tools. For many working forces in the production field, to settle the on-line quality issues, if available, any other methods than the numerical simulation tools would be recommended. The method using orthogonal array experiments can be considered as a first step for the process redesign and prerequisite for a necessary numerical simulation such as finite element thermal analysis (Figure 8), just as illustrared in the study.

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